Compact Low Power Avionics for the Europa Lander Concept and Other Missions to Ocean Worlds

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Abstract— ***This paper presents the results of NASA's game changing technology development entitled "Ultra Low Temperature Electronics" which represents a paradigm shift in spacecraft avionics development. The project has developed compact avionics technologies to address the Command & Data Handling (CDH), Power and Motor Control needs for mission concepts to ocean worlds such as a potential Europa Lander. We addressed this need by developing the key technologies necessary to develop a next generation compact avionics package. The key technologies that we developed significantly reduce the size, weight, power, and cost (SWAP-C) of the avionics package. These technologies will also allow extreme-environment missions to last longer in their environment by reducing the power and energy requirement to keep the avionics warm.***

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1. INTRODUCTION

The Ultra Low Temperature Electronics project has developed compact avionics technologies to address the Command & Data Handling (CDH), Power and Motor Control needs for mission concepts to ocean worlds such as a potential Europa Lander. The key technologies that we developed significantly reduce the size, weight, power, and cost (SWAP-C) of the avionics package. These technologies will also allow extreme-environment missions to last longer in their environment by reducing the power and energy requirement to keep the avionics warm.

The landed payload mass of ocean world missions typically require a spacecraft launch mass of 7-10 times the landed mass due to the required propellant to get payload to the surface. We addressed the mass challenge by developing standardized Multi-Chip Modules (MCMs), utilizing advanced connectors and System on a Chip technology. The outcome of this effort are proven technology developments that can be pulled together into a compact avionics package that is significantly lower SWAP-C compared to previously flown avionics assemblies.

This technology allows for a decrease in the volume (10x), and mass (3x) of electronic assemblies. The technology reduces the power (2x) by the use of an efficient processor and on-board power management. The energy required to keep the electronics warm is reduced by allowing the electronics to be stored at the ambient environment and heated prior to operation. This combination results in a unique high-density technology solution that extends the life of landed missions and allows mission planners to do more science through the mass and volume that is made available.

This work was divided into the following major thrust areas: Advanced Electronic Packaging, Low Power Computing, and Cold Capable Electronics. The results of this work were:

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1. Advanced Electronic Packaging (Key modules for a 3U Motor Controller Card)
2. Low Power Computing (Single Board Command and Data Handling System)
3. Cold Survivable Electronics (Eliminates the need for survival heating)

2. PROJECT GOAL

The project's goal is to allow a potential Europa Lander to last longer on the surface or allow more room for additional science by reducing the volume, mass and power of its avionics and the amount of energy required to keep the avionics warm.

This goal would be achieved through the use of advanced electronic packaging, low power computing and cold capable electronics. As illustrated in Table 1, this technology allows for a decrease in the volume (10x), and mass (3x), of electronic assemblies through the use of advanced packaging technology. The technology reduces the power (2x) by the use of an efficient processor and on-board power management. The energy required to keep the electronics warm is reduced by allowing the electronics to be stored at the ambient environment and heated prior to operation. As illustrated in Table 2 the power required for survival heating is eliminated.

Baseline Lander Avionics				Tech Lander Avionics		
Mass	14.13	Kg	→	Mass	3.58	Kg
Volume	11250	cc		Volume	1159	cc
Power	26	W		Power	13.44	W

Table 1: Compact Ultra Low Temperature Electronics Goal

Baseline Lander Avionics				Tech Lander Avionics		
Surviaval	-55C to	+70C	→	Surviaval	-200C to	+70C

Table 2: Survival Temperature Goal

The benefits to the Europa Lander concept are decreased mass, volume and power required for heating of the electronics. The benefits include increased science return, lower mission cost and improved reliability. Science return is increased through the decrease in volume of the electronics allowing for more room for science instruments. The decrease in power of the electronics would allow the lander to last longer on the surface. Mission costs is addressed by eliminated the need for survival heaters on the surface and on the long transit to the Europa surface. Reliability is improved through the mass and volume reduction by freeing up space for a dual string system.

3. SYSTEM DESIGN

The goal of this effort is to come up with a system capable of meeting Command & Data Handling (CDH), Power and Motor Control needs for missions to ocean worlds such as the Europa Lander project. The Europa Lander baseline design uses a separate computing platform for each of the mission stages. A computer in the descent stage handles the real time operation of the system. This frees up the landed computer from handling the complex real time requirements necessary for the landing on the surface. This allows for a more compact landed compute capability aimed at meeting the needs once successfully landed on the surface. Our technology addresses this need.

This goal is achieved through the use of advanced electronic As illustrated in Figure 1, we met this need by developing a compact avionics platform based upon a 1U, 10cm x 10cm format. As illustrated in Figure 2, the landed computer system consists of the following cards: Computer Card, Motor Control Card x4, Telemetry Card, Power Distribution Card, and Power Conversion Card. The Computer Card along with modules necessary to develop the motor control card are the focus of this effort.

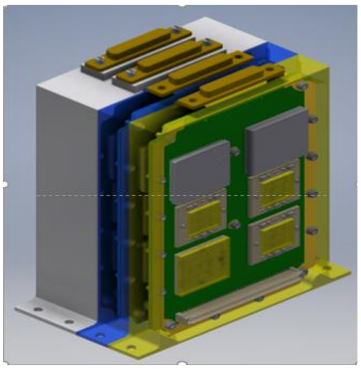

Figure 1: Packaging Concept

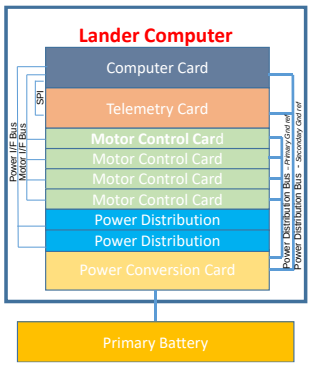

Figure 2: Europa Lander Concept Block Diagram

4. MINIATURIZED MOTOR CONTROL

Our electronics is now the baselined for the Europa Lander as a standalone motor controller. In this configuration we provide the motor control and motor control computation needs for the Europa Lander. This allowed the Europa Lander to take advantage of our mass and volume savings.

The miniaturized motor control assembly is based upon the computer card we developed and motor control modules. The current baseline is to use this box for motor control only. Lander CDH functions are handled by a more conventional processor. A block diagram of this system is shown in the following figure 3.

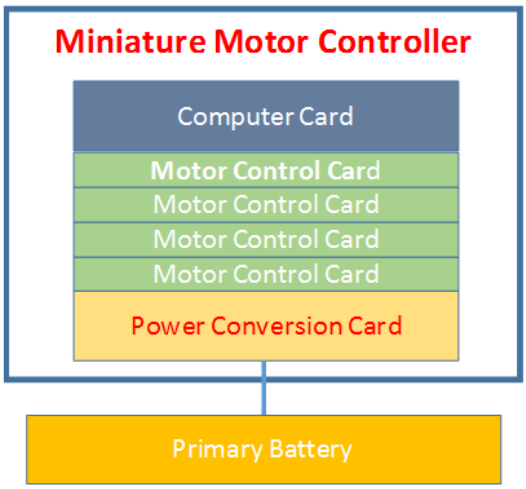

Figure 3: Stand Alone Motor Controller Block Diagram.

The packaging for this electronics package has been allowed to grow to increase the feasibility of the design. The boards have grown from 10cm x 10cm to 10cm x 16cm. This allows additional room to add circuitry as needed. An illustration of our packaging approach is shown in figure 4. Note the increased length from 10cm to 16cm.

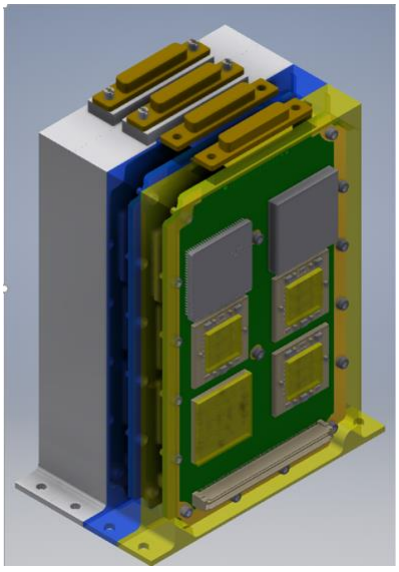

Figure 4: Stand Alone Motor Controller Packaging

As illustrated above Miniaturized Motor Controller, the packaging for this motor control assembly is based upon a slice based architecture originally developed for JPL's X2000 program [1]. The design utilized modules developed under this program to construct a Motor Control Card.

The block diagram of the motor control card is shown in Figure 5. The design consists of our computer card along with enough Motor Control Cards necessary to control 12 motors. Each motor card can control up to three motors. Only one motor can run at a time per card. Our design allows for the position of each motor to monitored by two resolvers, one motor shaft and one on the output of the gear box. Each resolver module can talk to 3 resolvers. Each card has two resolver modules. Each card has 2 resolver channels per motor. One for commutation and one for output position. Six in total. All can be running at any given time. There are four motor cards in the stack. This gives a total of 12 motors, and 24 resolver channels.

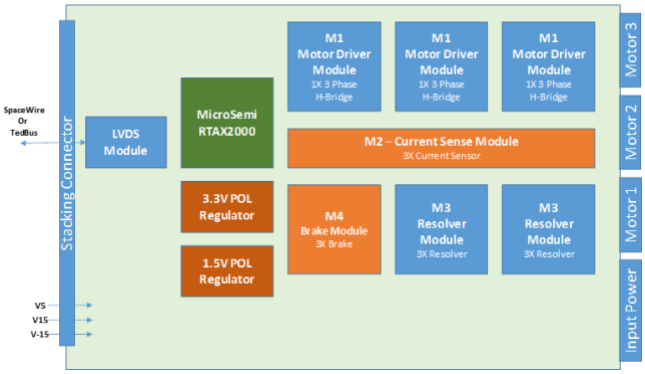

Figure 5: Motor Control Card Block Diagram

5. Advanced Electronic Packaging

We will utilized advanced packaging technology to achieve our goals for mass, and volume reductions. The primary technologies are the use of chip on board technology, high-density connectors, and a slice based design.

The substrate technology selected is the key enabler towards board density reduction. CoreEZ® a high-density substrate fabricated from thin particles containing organic laminates was the alternative to standard PWBs that contain glass cloth reinforced dielectrics. Figure 6 shows a cross-section comparison of i3's silica particle filled epoxy-based CoreEZ® thin laminate compared to a standard build up PWB. The absence of glass cloth in the dielectric provides several distinct key advantages including; reduction in thickness, tighter core via pitch, and improvements in assembly yields and reliability. The absence of the glass cloth also results in a smoother surface finish on the particle-filled dielectric, enabling higher resolution photolithography for finer line widths and spaces, and improved electrical performance, especially for high-speed

applications. [2] Laminate materials that do not contain glass cloth, unlike typical printed circuit board laminate materials, allow for the formation of smaller vias by UV laser drilling as opposed to more conventional vias formed by mechanical drilling of the glass cloth containing cores, and CO2 laser drilling of blind vias for interconnection in the buildup layers. The smaller via size minimizes capture pad area requirements and enables a much greater via density, resulting in substrate size reduction as compared to conventional PWB technology with glass cloth reinforcement.

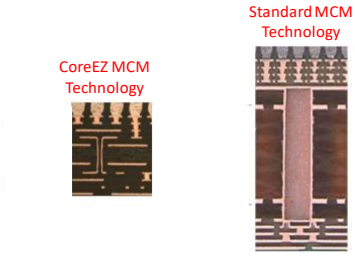

Figure 6: i3 CoreEZ® technology.

Another technology is the use of a high density connector. The connector that we have chosen is the verSI Series from AirBorn. This connector has ½ the pitch of the JPL flight standard micro-d connectors. This connector allows up to 4 times the number of conductors in the same number of space. Figure 7 illustrates this connector when applied on our computer card.

Figure 7: Illustration of AirBorn's verSI connector.

Under this development, two multi-chip modules were developed and on module from another program were utilized. They consists of a resolver module, a motor driver module and an LVDS interface. The Resolver Module illustrates an interface that requires many small components to implement. The Motor Driver is a module with high current requirements. The LDVS module, constructed under JPL Research and Technology Unibus effort is a communication interface module. [3]

The goal of this effort is to come up with a system capable of meeting Command & Data Handling (CDH), Power and Motor Control needs for missions to ocean worlds such as the Europa Lander project. The Europa Lander uses a separate computing platform for each of the mission stages. A computer in the descent stage handles the real time operation of the system. This frees up the landed computer from handling the complex real time requirements necessary for the landing on the surface. This allows for a more compact landed compute capability aimed at meeting the needs once successfully landed on the surface. Our technology addresses this need.

6. Motor Driver Module

The Motor Driver Module was the first module constructed under this effort. The module consists of the electronics necessary to drive a 3A brushless DC motor. This module consists of three MOSFET based half bridge drivers along with a radiation hardened MOSFET driver. The module consists of the MOSFET and driver die along with its associated discrete circuitry. The device was developed in partnership with i3 Technologies. JPL performed the electronic design and breadboard testing. i3 performed the detailed module design. Once constructed the modules were sent to JPL for testing.

The detailed module design was done by i3 Technologies. The design for the module is documented in the PDR package presented to JPL on April 28, 2016. [2] Actions for this review were addressed and presented at the M1 Module CDR held on May 28, 2016. The design done by i3 consisted of schematic entry, module layout, mechanical analysis, thermal analysis, and production setup. Figure 10 shows the completed module design along with a picture of module.

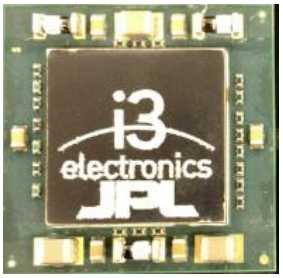

Figure 9: M1 Motor Driver Module.

In order to test the module Ground Support Equipment (GSE) needed to be developed. This GSE consisted of a socket developed by Ironwood Electronics custom designed for our module along with a test board. We designed our test board so that it can work around an "Elephant Trunk" type environmental unit. This unit allows us to test the unit under temperature while keeping the rest of the GSE at the ambient temperature.

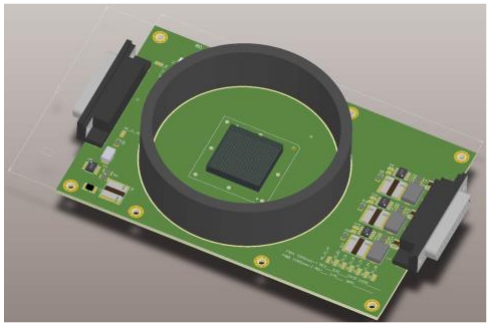

Figure 10: M1 Motor Driver Module Test Board

7. RESOLVER MODULE

The Resolver Module was the second module constructed under this effort. The module consists of the electronics necessary to implement three resolver interfaces. Resolvers are used to measure position of our motors. A resolver interfaces is allocated for shaft position both before and after the gear box. As illustrated in Figure 11, this module consists of excitation circuitry, input filter circuitry and the Analog To Digital Conversion circuitry to present the information to a FPGA for angle tracking processing. The device was developed in partnership with i3 Technologies. JPL performed the electronic design and breadboard testing. i3 performed the detailed module design. Once constructed the modules were sent to JPL for testing.

The detailed module design was done by i3 Technologies. The design for the module is documented in the PDR package presented to JPL on July 1, 2016. [3] Actions for this review were addressed and presented at the Module CDR held on August 2, 2016. The design done by i3 consisted of schematic entry, module layout, mechanical analysis, thermal analysis, and production setup. Figure 10 shows the completed module design along with a picture of module.

Figure 11: M1 Motor Driver Module.

In order to test the module Ground Support Equipment (GSE) needed to be developed. This GSE consisted of a socket developed by Ironwood Electronics custom designed for our module along with a test board. We designed our test board so that it can work around an "Elephant Trunk" type environmental unit. This unit allows us to test the unit under temperature while keeping the rest of the GSE at the ambient temperature.

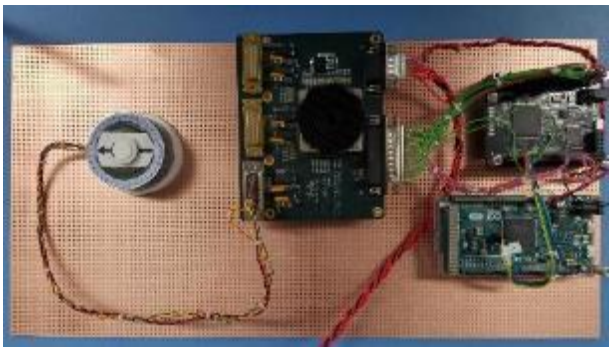

Figure 12: Resolver Module Test Board

8. LVDS MODULE

To implement the internal and external SpaceWire interfaces we are utilizing a LDVS (LOW VOLTAGE DIFFERENTIAL SWITCHING) module, constructed under the JPL Research and Technology Unibus effort. This module implements the physical layer of the SpaceWire Interfaces. As illustrated in the following figure, this module contains 2 Aeroflex SpaceWire interface receiver die along with two transmitter die. This component represents a 4X reduction in board area. The reduction in board area enabled by this device is key to allowing the computer card to fit on a single 10cm x 10cm card.

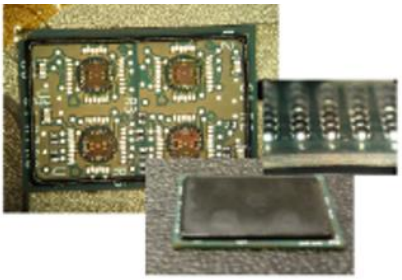

Figure 13: LVDS Module.

As illustrated in the following figure, an LVDS module test board was designed and constructed under this effort. This allowed us to address yield concerns, by allowing us to test the modules prior to installation on our computer card. The card was also used to temperature test the module. We were able to test one module. We found the module to work over the full operating temperature range of -55C to +125C on January 12, 2017.

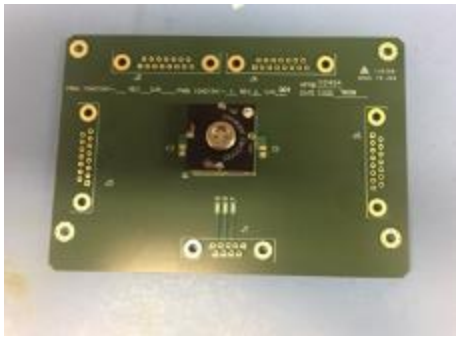

Figure 14: Resolver Module Test Board

9. Low Power Computing

A major development of this task is the development of single board (10cm x 10cm) Command and Data Handling System. This development started from the previously developed Sphinx development tailoring it to meet the needs for the Europa Lander computing requirements. The list that follows are key requirements for the computer card.

• The Computer Card shall be functioning under the following radiation requirements

- 300 Krads behind 100 mils of aluminum with a RDF of 2
- The Computer Card mass shall be less than 0.3 Kg
- The Computer Card dimensions shall fit an envelope of 100 mm x 100 mm 20 mm
- The average Computer Card power draw shall be less than 3W
- The Computer Card shall provide an EDAC protected NAND flash memory of 2 GBs for science and engineering telemetry
- The Computer Card shall be capable of interfacing with 4 cameras

We built our design based upon the Cobham Aeroflex GR712 processor. [4] We completed a detailed trade study on Febuary 8, 2017. A concept review for the computer card was held on April 08, 2016.[4] During this review we showed how we intended to meet our requirements along with the projected power, mass and volume.

Our computer design contains all the necessary interfaces along with the computer and its associated memory. A block diagram of the computing module is shown in the following figure. We have named this board Manx. The Manx board is an extreme-environment-capable compute element designed for operation on the surface of Europa (300 kRad TID). It is based on a dual-core LEON3FT SPARC processor, the Gaisler GR712 (datasheet). The Manx also includes a Microsemi RTG4, radiation-hardened FPGA and supports 5 spacewire links, 5 motor control links, 2 UARTs, Ethernet, CameraLink (for 30fps @ 4k resolution video), GPIO, I2C, SPI, and a housekeeping suite. The RTG4 supervises the processor and provides a 50MHz clock, resets, and access to peripheral interfaces. Manx is equipped with 8GBytes of science data storage, 400MBytes of SDRAM for the processor, and dual-redundant 128KByte EEPROM devices swapable through the FPGA. Manx operates off a 5V spacecraft bus and generates internal power through on-board point-of-load regulators.

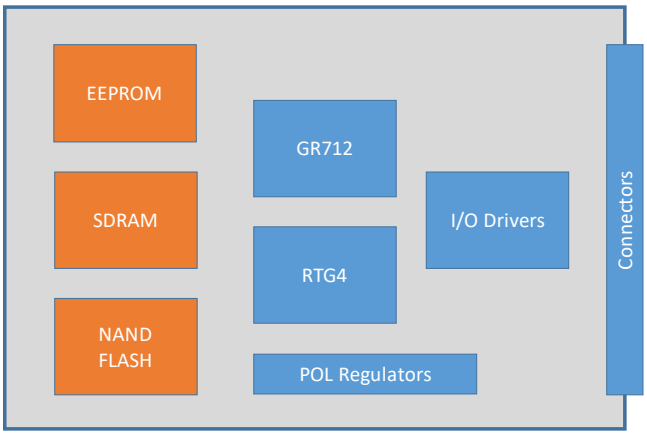

Figure 15: Computer Card Block Diagram.

The board was laid out through a JPL MEDALS contract with a company called Sierra Lobo. This board is the most complex, and densest board JPL has done for a C&DH board. The following figures illustrates an example of the wiring density.

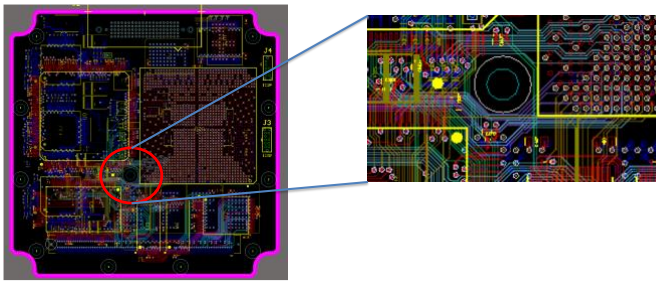

Figure 16: Illustration of Computer Card Wiring Density.

Figure 17: Completed Computer Card – Front

Figure 18: Completed Computer Card – Back

10. COLD CAPABLE ELECTRONICS

Work in the area of cold cable electronics consisted of three major thrust areas. The first was cryogenic testing of key components. The second area was thermal cycle testing of packages representative of the type of packages we envision using on the Europa Lander. The third area was recommendation of design rules for cryogenic temperature cycles.

11. CRYOGENIC DAISY CHAIN SOLDER TESTING WITH COTS COMPONENTS

Given the emphasis of new packaging technologies needed for this effort, our first focus from a cryogenic reliability point of view was to determine performance of various solders and other DUT attachment materials to various substrates.

There is a well-established ductile to brittle phase transition that occurs for a variety of solder compositions as temperatures are reduced to near cryogenic values [6]. Such a phase transition could impact our long-term reliability performance. We needed to quantify these types of materials changes using a variety of different adhesive technologies to ensure that we can meet our design goals.

To accomplish this, we developed a test matrix of two types of Pb based solder along with a conductive epoxy compound (Ablestick). This will allow us to performance long term cryogenic temperature cycling to study adhesive and mechanical strength parameters. We leverage existing commercial off the shelf (COTS) daisy chain DUTs and boards for our test vehicles. This test utilized COTS daisy chain boards from Practical Components (PC009 and PC012 models) and TB4 board from Omni as test beds. The final test matrix is shown in Table 3..

Board #	Ablestik adhesive	Eutectic Solder(63/37)	88/10/2 Solder
PC009-1	Y		
PC009-2		Y	
PC009-3			Y
PC012-1	Y		
PC012-2		Y	
PC012-3			Y
TB4-1	Y		
TB4-2		Y	
TB4-3			Y

Table 3: Board types and construction methods

Figure 19: Standardized Daisy Cain Test Boards

Both solder composition showed 60-70% reduction in resistance as a function of temperature down to -180C. Additional temperature cycles resulted in several Ablestick devices actually delaminating from the board entirely.

We investigated these Abelstick failures and determined the primary issue was workmanship with respect to the overall epoxy attach process. We also concluded that the high lead solder process temperatures where inadequate for this solder type. Additional DUT style, solder and substrate testing is planned. We are also testing final complete motor controller modules for cryogenic performance directly.

Figure 20 highlights some of the test results of the test matrix. During the first downward temperature ramp one of the Ablestick devices (DIP16) and one of the 88/10 solder devices (QPF44) failed.

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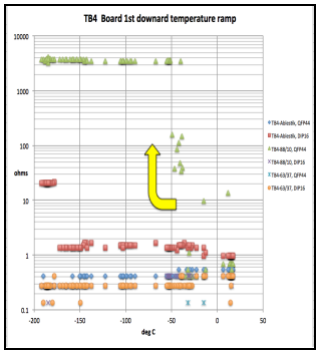

Figure 20: Daisy Chain Resistance vs. Temperature

12. CRYOGENIC TESTING OF I3 COREEZ SUBSTRATE

Tests were conducted to test the effectiveness of the i3 CoreEZ substrate / ENEPIG finish / Gold and Aluminum wire bonds, see test configuration figure 23. Tests of the substrate showed No anomalies found over the temperature ranges 25C to 0C to -50C to -100C to -150C to -180C with (20 hr soak) back to 25C (15 dwell @ each temperature). For this test the pass criteria was no more than a 20% increase in resistance at a specific temperature.

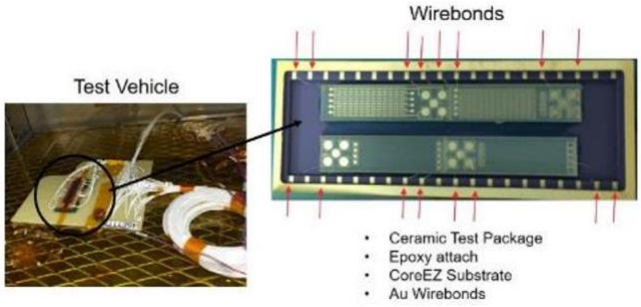

Figure 21: Illustration of CoreEZ substrate testing

13. EARLY CRYOGENIC TESTING OF STANDARD POLYIMIDE SUBSTRATES WITH ENEPIG FINISH AND AU AND ALUMINUM 1MIL WIRE BONDS

TCRE (thermal cycle resistant electronics) efforts at JPL have qualified Electrolytic Au with gold and aluminum wire bonding to survive Martian environments using conventional polyimide substrate. A new SOA commercially available finish is required to achieve fabrication of fine features need for MCM solutions. ENEPIG was selected. [5]

Attributes: PWB Finish: The key advantages of Electroless Nickel, Electroless Palladium, and Immersion Gold (ENEPIG) [2] finish plating are good planarity characteristics for attachment of the BGA/LGA COTS parts selected and elimination of black pad concerns. Black pad, or hyper-galvanic corrosion of electroless nickel during immersion gold plating, cannot occur with ENEPIG due to the protective palladium layer between the nickel and the gold. Additionally, the presence of palladium self-limit the gold plating thickness thereby eliminating the risk of excessive gold in solder. ENEPIG simplifies the process for chip-on-board (CoB) designs allowing wire bonding and solder technologies on an assembly with a single finish.

After 500 thermal cycle (–55°C to 125°C) and 250 thermal cycles (–130°C to 85°C), no destructive wire bond pull test per MIL-STD-883 for 1 mil wire was observed to have

values below the average pull strength minus three times the standard deviation or less than 3.0 grams.

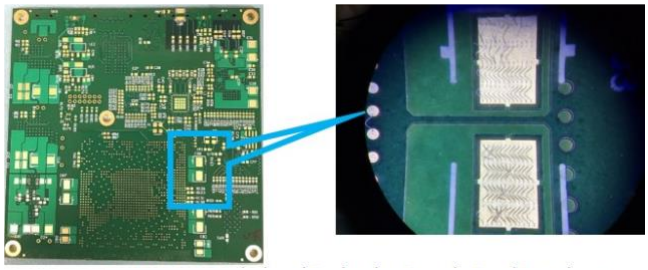

Figure 22: ENIPIG Wirebond Evaluation Sample Bond Locations

14. SUMMARY

Our LDVS, Motor Driver and Resolver Modules have all been design, built and tested over the Mil-Spec. temperature ranges. These modules are ready to be incorporated into future designs for the potential Europa Lander and other missions. Our computer card has been built and tested in an ambient temperature. The only issue with respect to the computer card is the radiation performance of the RTG4 FPGA and SDRAM. We have planned our activities to parallel the work going on with the Europa Mission. The Europa mission is using SRAM in place of SDRAM and either the Xilinx V5 or the Microsemi RTAX for its FPGA. To be usable for the Europa Lander the Computer Card would need to be modified to incorporate these 300KRad capable devices.

There are two main areas of infusion for our technology. Our avionics package is the baseline for motor control for the Europa Lander concept. Another venue for infusion is through the selected COLDTECH proposal "Cold Survivable Distributed Motor Controller".

The potential Europa Lander delivery would include our motor control modules packaged into a motor control card along with our computer card.

A NASA funded COLDTECH task called COLD SURVIVABLE DISTRIBUTED MOTOR CONTROLLER (CSDMC) will use our motor control modules as the basis for developing a motor control package capable of controlling one motor and packaged small enough to be distributed at the motors.

15. ACKNOWLEDGEMENT

The research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration

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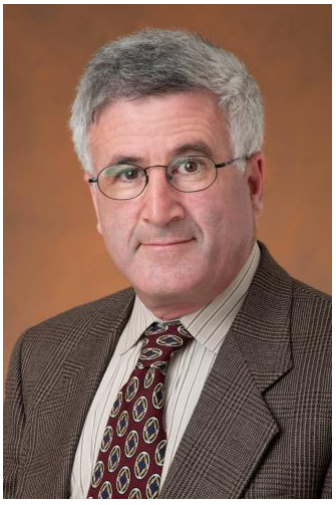
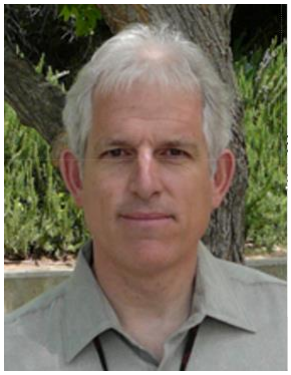


Gary Bolotin received a M.S. in Engineering from University of Illinois at Urban Champaign in 1985 and a B.S. in Engineering from Illinois Institute of Technology in 1984. He has been with JPL for more than 32 years. He is currently the lead of the Europa Lander Motor Controller. He has also managed engineering teams as both team leads and line manager at the section and group level,

Don Hunter has been with the Jet Propulsion Laboratory and a member of the Advanced Electronic Packaging Engineering section since 1993. Major contributions include; development of ruggedized 6U-VME fight system design for the Mars Pathfinder Mission, holds several Cal Tech and US Patents for work in advanced packaging systems architectures He holds a B.S. in mechanical engineering/Industrial Design from California State University Los Angeles and has been involved in the electro-mechanical packaging environment for over 28 years. He possesses experience ranging from commercial applications of deck top test equipment to military (DOD) cold temperature and high-G integrated packaging applications.



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